Freeform Search

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term:

L18 and (bipolar)

Display: 10 **Documents in** Display Format: - **Starting with Number** 1

Generate: ○ Hit List ◉ Hit Count ○ Side by Side ○ Image

Search | Clear | Interrupt

Search History

DATE: Thursday, January 05, 2006 Printable Copy   Create Case

Set Name	Query	Hit Count	Set Name
side by side			result set
	DB=USPT; PLUR=YES; OP=ADJ		
L19	L18 and (bipolar)	1	L19
L18	6736540.pn.	1	L18
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L17	(thermal sens$5 transistors) adj5 (integrated circuit or IC or wafer)	0	L17
L16	thermal sens$5 transistors adj5 chip	0	L16
L15	temperature sens$5 transistors adj5 chip	7	L15
L14	temperature measur$3 transistors adj5 IC	0	L14
L13	temperature sens$5 transistors adj5 IC	2	L13
L12	temperature sens$4 transistors adj5 IC	2	L12
	DB=EPAB; PLUR=YES; OP=ADJ		
L11	KR-2003042942-A.did.	0	L11
L10	KR-434237-B.did.	0	L10
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L9	temperature sens$4 transistors adj5 integrated circuit	3	L9
L8	transistors adj5 integrated circuit	21414	L8
L7	transistors on IC	0	L7

L6	L1 and (Vbe)	33	L6
L5	L2 and (Vbe)	1	L5
L4	L3 and (Vbe)	5	L4
L3	L1 and (second transistor)	109	L3
L2	L1 and (plurality transistors or plurality semiconductors)	74	L2
L1	374/$.ccls.	28913	L1

END OF SEARCH HISTORY

Freeform Search

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term:
L72 and (transistor)

Display: 10 Documents in **Display Format:** Starting with Number 1
Generate: O Hit List ⦿ Hit Count O Side by Side O Image

Search | Clear | Interrupt

Search History

DATE: Thursday, January 05, 2006 Printable Copy Create Case

Set Name Query
side by
side

DB=PGPB,USPT,USOC,EPAB,JPAB; PLUR=YES; OP=ADJ

L73 L72 and (transistor)
L72 L68 and (plurality thermal sensors)
L71 L68 and (plurality sens$5 diodes)
L70 L68 and (plurality sens$5 transistors)
L69 L68 and (plurality sens$4 transistors)
L68 L67 and (IC or integrated circuit or chip or wafer)
L67 (374/170,172,178,141,137,166,163;327/493,504,505,512,513;361/103,365/212,211;324/760,765, [CCLS]

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

L66 simultaneously obtain$3 temperature different locations
L65 simultaneously acces$4 temperature different locations
L64 simultaneously sens$3 temperature different locations
L63 simultaneously measur$3 temperature different locations
L62 simultaneously measure temperature different locations
L61 L60 and (IC or integrated circuit or chip or wafer or temperature or thermal)

L60 (plurality sens$3 transistors)

L59 (plurality sens$3 trnsistors) and (IC or chip or integrated circuit or wafer)

L58 L40 and (plurality sens$3 transistors)

L57 L54 and (plurality sensing transistors)

L56 L54 and (plurality locations)

L55 L54 and (different locations)

L54 L52 and (simultaneous$2)

L53 L52 and (simultaneous$2 temperature)

L52 L40 and (chip or IC or intergrated circuit or wafer)
  DB=PGPB; PLUR=YES; OP=ADJ

L51 L49 and (n-1)

L50 L49 and (individually or selectively or simultaneously)

L49 20040001527

L48 L44 and (selectively or simultaneously)

L47 L44 and (independently)

L46 L44 and (N-1)

L45 L44 and (n-1)

L44 20040005127
  DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

L43 L2 and (npn adj5 pnp)

L42 L40 and (npn adj5 pnp)

L41 L40 and (parallel transistors)

L40 374/$.ccls.

L39 parallel transistors

L38 parallel npn pnp

L37 parallel pnp npn

L36 transistor invers$3 parallel transistor

L35 L34 same (inverse parallel)

L34 transistor connection

L33 L31 and (pins or access points)

L32 L31 and (n pins)

L31 L30 same (transistors)

L30 inverse parallel

L29 (inverse parallel) same (transistors) samw (pin$1)

L28 inverse parallel transistors

L27 inverse transistor$1 pair

L26 inverse pair$1 transistor$1

L25 L24 and (n pins)

L24 n(n-1)

L23 n(n-1) pairs

L22 L21 and (temperature or thermal)

L21 L20 and (pins)
L20 L19 and (transistors)
L19 257/48
L18 L16 and (temperature or thermal)
L17 L15 and (n pins)
L16 L15 and (pins)
L15 L14 and (transistors)
L14 L13 and (transistors or semiconductors)
L13 438/14
L12 L9 and (pins)
L11 L7 and (n pins)
L10 L9 and (n pins)
L9   L7 and (transistors)
L8   L7 and (antiparallel transistors)
L7   438/18
L6   L2 and (inverse connection)
L5   L2 and (antiparallel)
L4   L3 and (antiparallel)
L3   L2 and (transistor$1)
L2   327/512
L1   antiparallel transistors

END OF SEARCH HISTORY